TMS 2600 JC, TMS 2600 NC
2048-BIT STATIC READ-ONLY MEMORY

JANUARY, 1971

features

- 2048-bit capacity
- Static operation
- Maximum access time under 1 microsecond
- Two organizations available
- Open-drain output buffers or double-ended buffers
- TTL compatible
- 24-pin dual-in-line package

description

The TMS 2600 JC/NC series is a family of static read-only memories,each with capacity of 2048 bits.

Programming the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

Inputs are available for enabling the chip and for selecting between a memory organization of 512 words of four bits or 256 words of eight bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground (substrate).

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

"TMS 2600 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 2600 NC" is used for a unit mounted in a 24-pin plastic package.

logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2600 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times. Access time is defined as the time between a change of data on any logic input or chip select line and a change of data on the output of a TTL gate. (See switching circuit).

operation (continued)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

organizational control logic

		OUTPUTS	
		B_1 B_3 B_5 B_7	B_2 B_4 B_6 B_8
256 words of 8 bits (MC = Logical 0):	A_9 = Logical 1	Enabled	Enabled
512 words of 4 bits (MC = Logical 1):	A_9 = Logical 0	Enabled	Logical 1
	A_9 = Logical 1	Logical 1	Enabled

To use the device as a 512 words of 4 bits, connect B_1 to B_2, B_3 to B_4, B_5 to B_6, B_7 to B_8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−16	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−16	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	650			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

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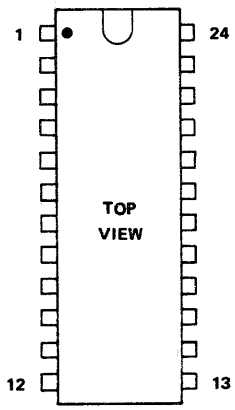
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Notes 1 and 3)	See switching circuit		600	1000	ns
t_{A2}	Access time (Notes 1 and 3)	See switching circuit		550	1000	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		180		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		15		mA
I_{GG}	Gate current			1.0		μA

NOTES: 1. Open drain buffer
2. Push-pull buffer
3. See Switching Diagram
4. Either open-drain or push-pull configuration

mechanical data and pin configuration

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2600 JC) and a 24-pin plastic package (TMS 2600 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	13	A_9
2	A_2	14	CS
3	A_1	15	MC
4	B_1	16	V_{GG}
5	B_2	17	A_8
6	B_3	18	A_7
7	B_4	19	A_6
8	B_5	20	A_5
9	B_6	21	A_4
10	B_7	22	NC
11	B_8	23	NC
12	V_{SS}	24	V_{DD}

A – input
B – output
MC – mode control
CS – chip select

V_{DD} – drain power supply
V_{GG} – ground power supply
V_{SS} – substrate

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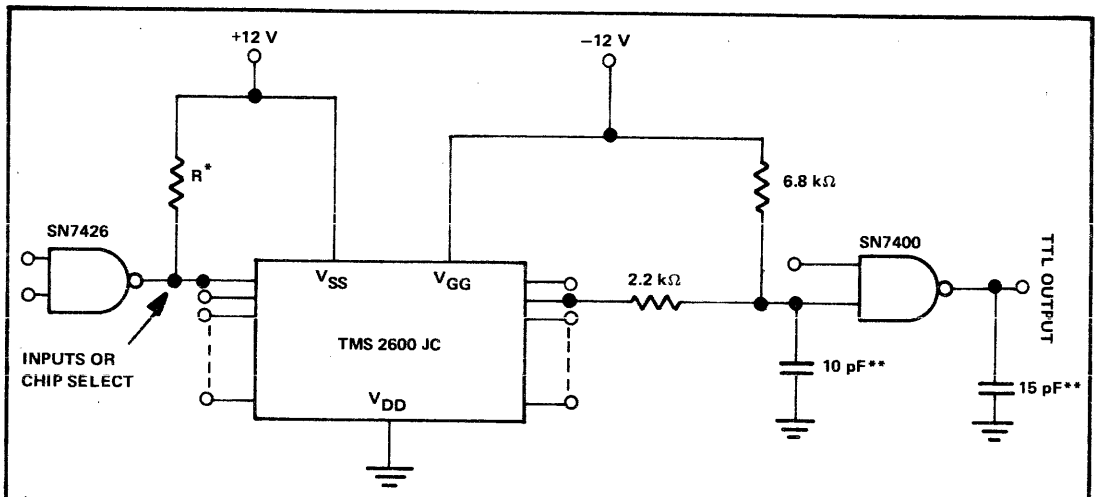
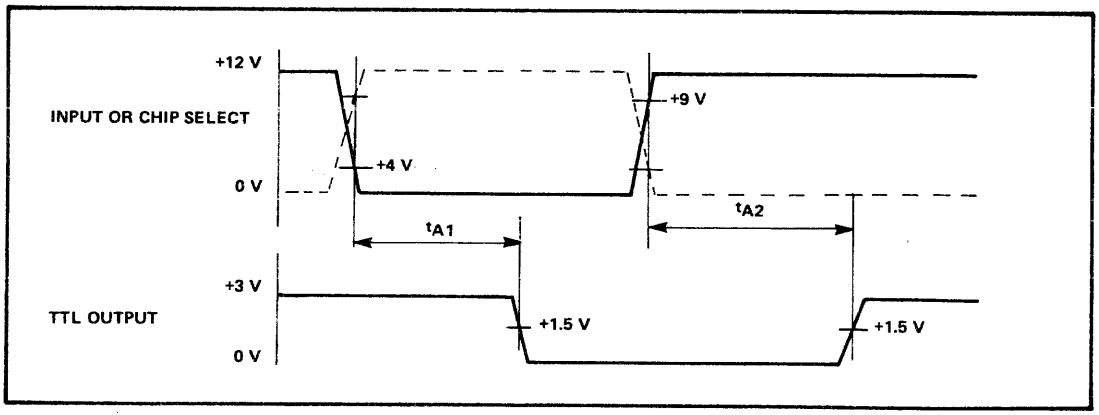
switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram



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off the shelf devices

These devices have been programmed by TI and are available off the shelf:

1) TMS 2601 JC/NC

   This device has been programmed to demonstrate the capabilities of the TMS 2600 JC/NC series. It is used as a sample device. The buffers are single ended.

2) TMS 2602 JC/NC Code Converter

   This device converts the USASCII code into the selectric line code and vice versa.

3) TMS 2603 JC/NC Code Converter

   This device converts the full EBCDIC code into the USASCII code.

Truth tables for the TMS 2602 JC/NC and 2603 JC/NC are available upon request.

TRUTH TABLE, TMS 2601 JC/NC

INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1
0	1	1	1	1	1	1	1	1	64	1	1	1	1	1	1	0	0	128	1	1	1	1	0	0	0	0	192	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	65	1	1	1	1	1	1	0	0	129	1	1	1	1	0	0	0	0	193	1	1	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1	66	1	1	1	1	1	1	0	0	130	1	1	1	1	0	0	0	0	194	1	1	0	0	0	0	0	0
3	1	1	1	1	1	1	1	1	67	1	1	1	1	1	1	0	0	131	1	1	1	1	0	0	0	0	195	1	1	0	0	0	0	0	0
4	1	1	1	1	1	1	1	1	68	1	1	1	1	1	1	0	0	132	1	1	1	1	0	0	0	0	196	1	1	0	0	0	0	0	0
5	1	1	1	1	1	1	1	1	69	1	1	1	1	1	1	0	0	133	1	1	1	1	0	0	0	0	197	1	1	0	0	0	0	0	0
6	1	1	1	1	1	1	1	1	70	1	1	1	1	1	1	0	0	134	1	1	1	1	0	0	0	0	198	1	1	0	0	0	0	0	0
7	1	1	1	1	1	1	1	1	71	1	1	1	1	1	1	0	0	135	1	1	1	1	0	0	0	0	199	1	1	0	0	0	0	0	0
8	1	1	1	1	1	1	1	0	72	1	1	1	1	1	0	0	0	136	1	1	1	0	0	0	0	0	200	1	0	0	0	0	0	0	0
9	1	1	1	1	1	1	1	0	73	1	1	1	1	1	0	0	0	137	1	1	1	0	0	0	0	0	201	1	0	0	0	0	0	0	0
10	1	1	1	1	1	1	1	1	74	1	1	1	1	1	1	0	0	138	1	1	1	1	0	0	0	0	202	1	1	0	0	0	0	0	0
11	1	1	1	1	1	1	1	1	75	1	1	1	1	1	1	0	0	139	1	1	1	1	0	0	0	0	203	1	1	0	0	0	0	0	0
12	1	1	1	1	1	1	1	1	76	1	1	1	1	1	1	0	0	140	1	1	1	1	0	0	0	0	204	1	1	0	0	0	0	0	0
13	1	1	1	1	1	1	1	1	77	1	1	1	1	1	1	0	0	141	1	1	1	1	0	0	0	0	205	1	1	0	0	0	0	0	0
14	1	1	1	1	1	1	1	1	78	1	1	1	1	1	1	0	0	142	1	1	1	1	0	0	0	0	206	1	1	0	0	0	0	0	0
15	1	1	1	1	1	1	1	1	79	1	1	1	1	1	1	0	0	143	1	1	1	1	0	0	0	0	207	1	1	0	0	0	0	0	0
16	1	1	1	1	1	1	1	0	80	1	1	1	1	1	0	0	0	144	1	1	1	0	0	0	0	0	208	1	0	0	0	0	0	0	0
17	1	1	1	1	1	1	1	0	81	1	1	1	1	1	0	0	0	145	1	1	1	0	0	0	0	0	209	1	0	0	0	0	0	0	0
18	1	1	1	1	1	1	1	0	82	1	1	1	1	1	0	0	0	146	1	1	1	0	0	0	0	0	210	1	0	0	0	0	0	0	0
19	1	1	1	1	1	1	1	0	83	1	1	1	1	1	0	0	0	147	1	1	1	0	0	0	0	0	211	1	0	0	0	0	0	0	0
20	1	1	1	1	1	1	1	1	84	1	1	1	1	1	1	0	0	148	1	1	1	1	0	0	0	0	212	1	1	0	0	0	0	0	0
21	1	1	1	1	1	1	1	1	85	1	1	1	1	1	1	0	0	149	1	1	1	1	0	0	0	0	213	1	1	0	0	0	0	0	0
22	1	1	1	1	1	1	1	1	86	1	1	1	1	1	1	0	0	150	1	1	1	1	0	0	0	0	214	1	1	0	0	0	0	0	0
23	1	1	1	1	1	1	1	1	87	1	1	1	1	1	1	0	0	151	1	1	1	1	0	0	0	0	215	1	1	0	0	0	0	0	0
24	1	1	1	1	1	1	1	0	88	1	1	1	1	1	0	0	0	152	1	1	1	0	0	0	0	0	216	1	0	0	0	0	0	0	0
25	1	1	1	1	1	1	1	0	89	1	1	1	1	1	0	0	0	153	1	1	1	0	0	0	0	0	217	1	0	0	0	0	0	0	0
26	1	1	1	1	1	1	1	0	90	1	1	1	1	1	0	0	0	154	1	1	1	0	0	0	0	0	218	1	0	0	0	0	0	0	0
27	1	1	1	1	1	1	1	0	91	1	1	1	1	1	0	0	0	155	1	1	1	0	0	0	0	0	219	1	0	0	0	0	0	0	0
28	1	1	1	1	1	1	1	0	92	1	1	1	1	1	0	0	0	156	1	1	1	0	0	0	0	0	220	1	0	0	0	0	0	0	0
29	1	1	1	1	1	1	1	0	93	1	1	1	1	1	0	0	0	157	1	1	1	0	0	0	0	0	221	1	0	0	0	0	0	0	0
30	1	1	1	1	1	1	1	1	94	1	1	1	1	1	1	0	0	158	1	1	1	1	0	0	0	0	222	1	1	0	0	0	0	0	0
31	1	1	1	1	1	1	1	1	95	1	1	1	1	1	1	0	0	159	1	1	1	1	0	0	0	0	223	1	1	0	0	0	0	0	0
32	1	1	1	1	1	1	1	0	96	1	1	1	1	1	0	0	0	160	1	1	1	0	0	0	0	0	224	1	0	0	0	0	0	0	0
33	1	1	1	1	1	1	1	0	97	1	1	1	1	1	0	0	0	161	1	1	1	0	0	0	0	0	225	1	0	0	0	0	0	0	0
34	1	1	1	1	1	1	1	0	98	1	1	1	1	1	0	0	0	162	1	1	1	0	0	0	0	0	226	1	0	0	0	0	0	0	0
35	1	1	1	1	1	1	1	0	99	1	1	1	1	1	0	0	0	163	1	1	1	0	0	0	0	0	227	1	0	0	0	0	0	0	0
36	1	1	1	1	1	1	1	0	100	1	1	1	1	1	0	0	0	164	1	1	1	0	0	0	0	0	228	1	0	0	0	0	0	0	0
37	1	1	1	1	1	1	1	0	101	1	1	1	1	1	0	0	0	165	1	1	1	0	0	0	0	0	229	1	0	0	0	0	0	0	0
38	1	1	1	1	1	1	1	0	102	1	1	1	1	1	0	0	0	166	1	1	1	0	0	0	0	0	230	1	0	0	0	0	0	0	0
39	1	1	1	1	1	1	1	0	103	1	1	1	1	1	0	0	0	167	1	1	1	0	0	0	0	0	231	1	0	0	0	0	0	0	0
40	1	1	1	1	1	1	0	0	104	1	1	1	1	1	0	0	0	168	1	1	0	0	0	0	0	0	232	0	0	0	0	0	0	0	0
41	1	1	1	1	1	1	0	0	105	1	1	1	1	1	0	0	0	169	1	1	0	0	0	0	0	0	233	0	0	0	0	0	0	0	0
42	1	1	1	1	1	1	1	0	106	1	1	1	1	1	0	0	0	170	1	1	1	0	0	0	0	0	234	1	0	0	0	0	0	0	0
43	1	1	1	1	1	1	1	0	107	1	1	1	1	1	0	0	0	171	1	1	1	0	0	0	0	0	235	1	0	0	0	0	0	0	0
44	1	1	1	1	1	1	1	0	108	1	1	1	1	1	0	0	0	172	1	1	1	0	0	0	0	0	236	1	0	0	0	0	0	0	0
45	1	1	1	1	1	1	1	0	109	1	1	1	1	1	0	0	0	173	1	1	1	0	0	0	0	0	237	1	0	0	0	0	0	0	0
46	1	1	1	1	1	1	1	0	110	1	1	1	1	1	0	0	0	174	1	1	1	0	0	0	0	0	238	1	0	0	0	0	0	0	0
47	1	1	1	1	1	1	1	0	111	1	1	1	1	1	0	0	0	175	1	1	1	0	0	0	0	0	239	1	0	0	0	0	0	0	0
48	1	1	1	1	1	1	0	0	112	1	1	1	1	1	0	0	0	176	1	1	0	0	0	0	0	0	240	0	0	0	0	0	0	0	0
49	1	1	1	1	1	1	0	0	113	1	1	1	1	1	0	0	0	177	1	1	0	0	0	0	0	0	241	0	0	0	0	0	0	0	0
50	1	1	1	1	1	1	0	0	114	1	1	1	1	1	0	0	0	178	1	1	0	0	0	0	0	0	242	0	0	0	0	0	0	0	0
51	1	1	1	1	1	1	0	0	115	1	1	1	1	1	0	0	0	179	1	1	0	0	0	0	0	0	243	0	0	0	0	0	0	0	0
52	1	1	1	1	1	1	1	0	116	1	1	1	1	1	0	0	0	180	1	1	1	0	0	0	0	0	244	1	0	0	0	0	0	0	0
53	1	1	1	1	1	1	1	0	117	1	1	1	1	1	0	0	0	181	1	1	1	0	0	0	0	0	245	1	0	0	0	0	0	0	0
54	1	1	1	1	1	1	1	0	118	1	1	1	1	1	0	0	0	182	1	1	1	0	0	0	0	0	246	1	0	0	0	0	0	0	0
55	1	1	1	1	1	1	1	0	119	1	1	1	1	1	0	0	0	183	1	1	1	0	0	0	0	0	247	1	0	0	0	0	0	0	0
56	1	1	1	1	1	1	0	0	120	1	1	1	1	1	0	0	0	184	1	1	0	0	0	0	0	0	248	0	0	0	0	0	0	0	0
57	1	1	1	1	1	1	0	0	121	1	1	1	1	1	0	0	0	185	1	1	0	0	0	0	0	0	249	0	0	0	0	0	0	0	0
58	1	1	1	1	1	1	0	0	122	1	1	1	1	1	0	0	0	186	1	1	0	0	0	0	0	0	250	0	0	0	0	0	0	0	0
59	1	1	1	1	1	1	0	0	123	1	1	1	1	1	0	0	0	187	1	1	0	0	0	0	0	0	251	0	0	0	0	0	0	0	0
60	1	1	1	1	1	1	0	0	124	1	1	1	1	1	0	0	0	188	1	1	0	0	0	0	0	0	252	0	0	0	0	0	0	0	0
61	1	1	1	1	1	1	0	0	125	1	1	1	1	1	0	0	0	189	1	1	0	0	0	0	0	0	253	0	0	0	0	0	0	0	0
62	1	1	1	1	1	1	1	0	126	1	1	1	1	1	0	0	0	190	1	1	1	0	0	0	0	0	254	1	0	0	0	0	0	0	0
63	1	1	1	1	1	1	1	0	127	1	1	1	1	1	0	0	0	191	1	1	1	0	0	0	0	0	255	1	0	0	0	0	0	0	0

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SOFTWARE PACKAGE

input format

Programming information for the TMS 2600 JC/NC should be transmitted to TI in the form of a DECK of 43 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI should be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the various circuit options desired will be transmitted on a special form supplied by TI.

The main memory array can be so programmed that for any binary input of A_8 through A_1 (0 to 255), the outputs B_8 through B_1 are uniquely determined. Since A_9 and MC are used to select output paths, the internal storage of data in the array is the same regardless of organization – 256 x 8 or 512 x 4.

Each card in the data deck describes the outputs for six or twelve input addresses, depending on whether eight or four outputs are desired. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

data card format

Column	
1-2	Punch the sequential card number (01 through 43)
3	Blank
4-5	Punch a "26" to signify TMS 2600 JC
6-11	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers)
12	Blank (a space for the revision letter if necessary)
13	Punch a "8" if using the 256 x 8 configuration, or punch a "4" if using the 512 x 4 configuration
14	Punch a "D" for open-drain type output buffers, or punch a "P" for push-pull type output buffers
15-17	Punch a right-justified integer representing the binary input address (0-255 if 8 outputs, 0-511 if only 4 outputs) for the first set of outputs described on the card
18	Punch a "–" (minus sign)
19-21	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card
22	Blank
23-80	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0

For a 256 x 8 configuration each card will describe 6 output sets. The 43rd card will contain only 4 output sets.

23-30	Punch the outputs desired for B_8, B_7, B_6, B_5, B_4, B_3, B_2, and B_1, in that order, for the first address specified on the card
33-40	Punch the outputs desired for the second address
43-50	Punch the outputs desired for the third address

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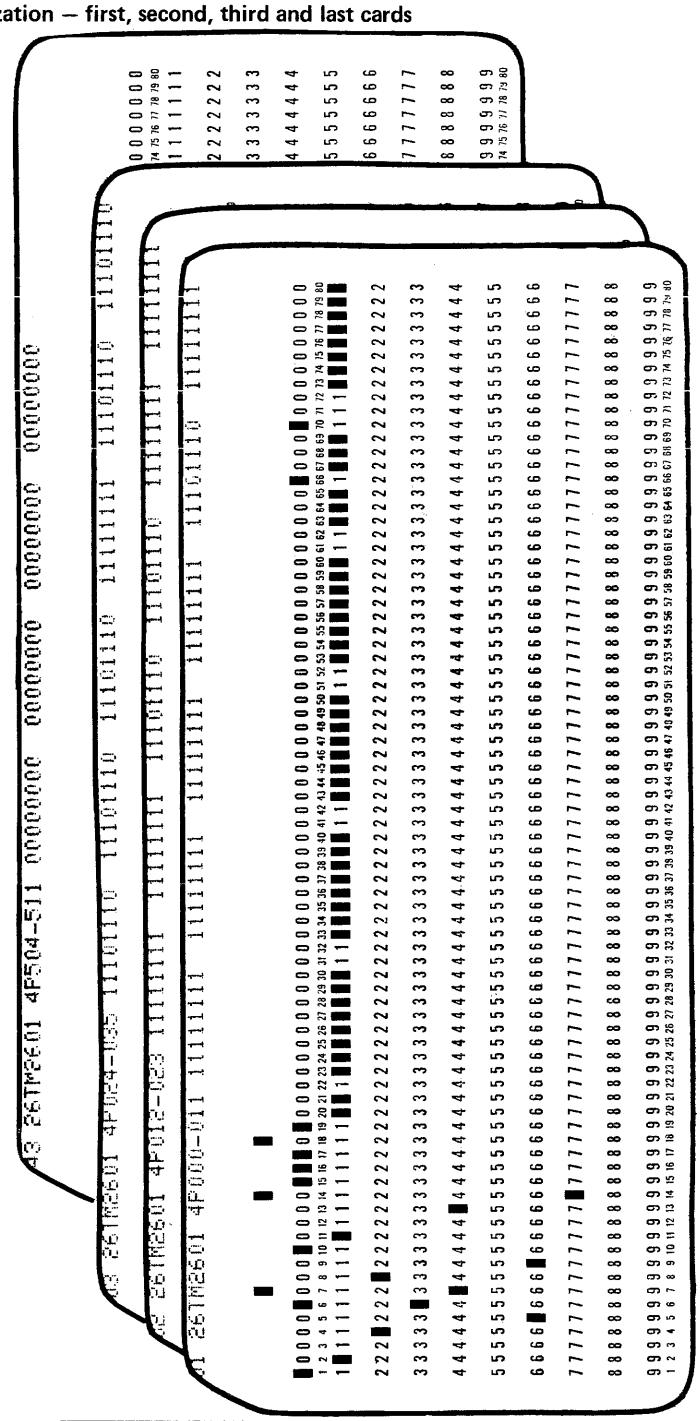
data card format (continued)

Column	
53-60	Punch the outputs desired for the fourth address
63-70	Punch the outputs desired for the fifth address
73-80	Punch the outputs desired for the sixth address

For a 512 x 4 configuration, each card will describe 12 output sets. The 43rd card will contain only 8 output sets.

23-26	Punch the outputs desired for B_8 or B_7, B_6 or B_5, B_4 or B_3, B_2 or B_1, in that order, for the first address specified on the card.
27-30	Punch the outputs desired for the second address
33-36	Punch the outputs desired for the third address
37-40	Punch the outputs desired for the fourth address
43-46	Punch the outputs desired for the fifth address
47-50	Punch the outputs desired for the sixth address
53-56	Punch the outputs desired for the seventh address
57-60	Punch the outputs desired for the eighth address
63-66	Punch the outputs desired for the ninth address
67-70	Punch the outputs desired for the tenth address
73-76	Punch the outputs desired for the eleventh address
77-80	Punch the outputs desired for the twelfth address

512 x 4 organization — first, second, third and last cards



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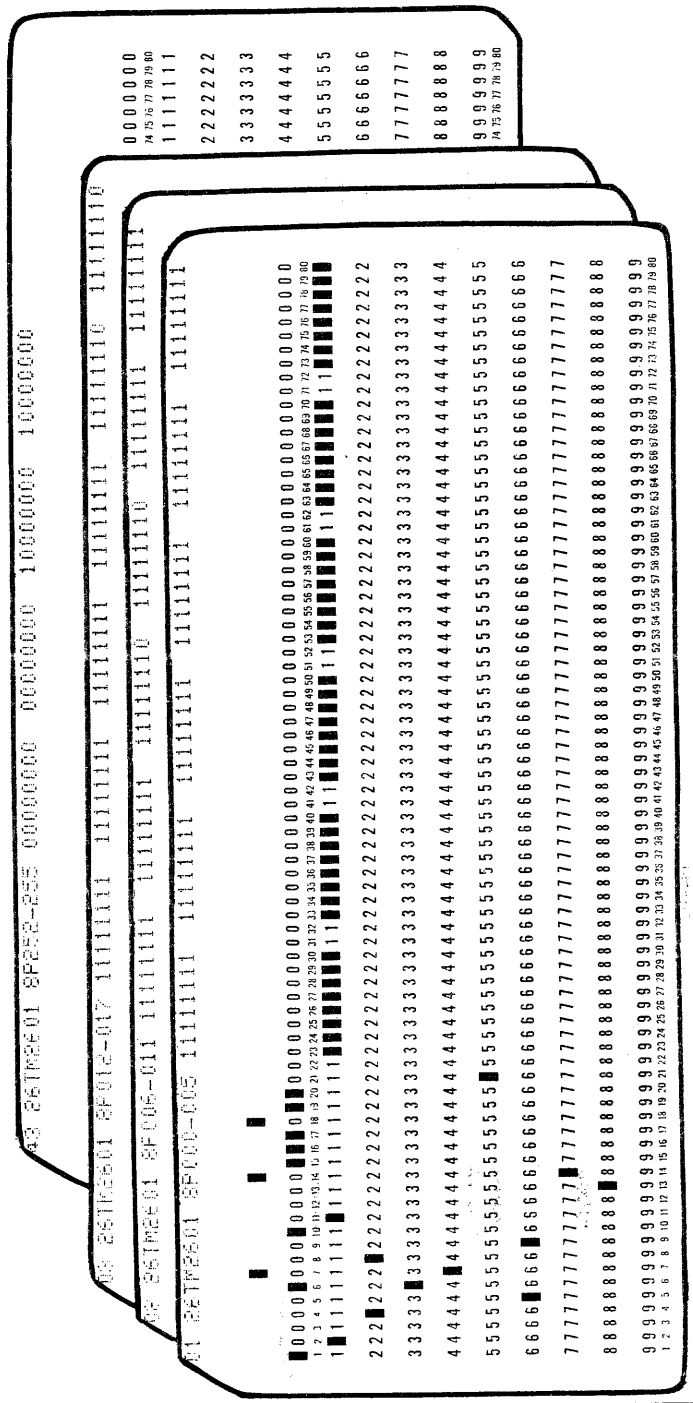
256 x 8 organization – first, second, third and last cards



TMS 2602 JC, TMS 2602 NC
USASCII-TO-SELECTRIC/SELECTRIC-TO-USASCII CODE CONVERTER

description

The TMS 2602 JC/NC is programmed TMS 2600 JC/NC ROM capable of converting both USASCII to Selectric Line Code, and Selectric Line Code to USASCII. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_7, and Outputs O_2 through O_8 of the ROM correspond to the two codes as follows:

ROM INPUT	SELECTRIC BIT	USASCII BIT	ROM OUTPUT
I_1	1	b_1	O_2
I_2	2	b_2	O_3
I_3	4	b_3	O_4
I_4	8	b_4	O_5
I_5	A	b_5	O_6
I_6	B	b_6	O_7
I_7	S	b_7	O_8

mode selection

Output O_1 is even parity for the 7-bit output word.

Input I_8 at logic 0 — USASCII is converted to Selectric Line Code

Input I_8 at logic 1 — Selectric Line Code is converted to USASCII

logic definition

As with the TMS 2600 JC/NC, negative logic is assumed.

Logical 1 = most negative voltage

Logical 0 = most positive voltage

code definition

The standard USASCII table is used as the USASCII code. The selectric code used is the IBM Correspondence Selectric Line Code. The following tables show the mapping from USASCII to Selectric and vice versa.

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